IN THE CLAIMS

1. (Currently Amended) A method for implementing a programmable chip system onto a printed circuit board, the method comprising:

receiving at a generator module customization information associated with a processor core and a plurality of programmable chip components;

configuring, at the generator module, the processor core and the plurality of programmable chip components for implementation on the programmable chip system, including creating a logic description and providing the logic description to a synthesis tool;

automatically determining voltage and ground pins associated with the programmable chip system;

~~providing a netlist, wherein~~ utilizing the generator module to automatically generate a netlist and automatically providing the netlist to a printed circuit board layout tool which uses the netlist to generate a layout coupling the processor core and the plurality of programmable chip components to off-chip components; and

utilizing one or more secondary side arbitrators with one or more of the plurality of programmable chip components, thereby enabling direct communication between a secondary component to which a secondary side arbitrator corresponds and a primary programmable chip component; and

wherein the processor core transmits request controls to the secondary side arbitrator corresponding to the secondary component.

2. (Original) The method of claim 1, wherein the netlist is a printer circuit board netlist.

3. (Currently Amended) The method of claim 2, wherein capacitors are bypassed for ground pins ~~pints~~ and voltage pins.

4. (Original) The method of claim 1, wherein the plurality of programmable chip components are received from a library.

5. (Original) The method of claim 1, wherein customization information includes parameterization information.

6. (Original) The method of claim 1, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

7. (Original) The method of claim 1, wherein the off-chip component is an external memory device.

8. (Original) The method of claim 1, wherein the off-chip component is an application specific standard product.

9. (Original) The method of claim 8, wherein the printed circuit board layout tool takes the netlist and generates schematic traces.

10. (Currently Amended) A system for implementing a programmable chip system ~~device~~, the system comprising:

a generator module having an interface operable to receive customization information associated with a processor core and a plurality of programmable chip components;

a processor operable to configure the processor core and the plurality of programmable chip components for implementation on the programmable chip and operable to create a logic description and provide the logic description to a synthesis tool, the processor configured to determine voltage and ground pins associated with the programmable chip system and to automatically generate a netlist and to provide a netlist to ~~a~~ printed circuit board layout tool, wherein the printed circuit board layout tool uses the netlist to generate a connection layout coupling the processor core and the plurality of programmable chip components to off-chip components; and

one or more secondary side arbitrators to enable direct communication between a secondary component and a primary programmable chip component, wherein the processor transmits request controls to the secondary side arbitrator corresponding to the secondary component.

11. (Original) The system of claim 10, wherein the netlist is a printer circuit board netlist.

12. (Currently Amended) The system of claim 11, wherein capacitors are bypassed for ground pins ~~pints~~ and voltage pins.

13. (Original) The system of claim 10, wherein the plurality of programmable chip components are received from a library.

14. (Original) The system of claim 13, wherein customization information includes parameterization information.

15. (Original) The system of claim 14, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

16. (Original) The system of claim 10, wherein the off-chip component is an external memory device.

17. (Original) The system of claim 10, wherein the off-chip component is an application specific standard product.

18. (Original) The system of claim 17, wherein the printed circuit board layout tool takes the netlist and generates schematic traces.

19. (currently amended) An apparatus for implementing a programmable chip system onto a printed circuit board, the apparatus comprising:

means for receiving at a generator module customization information associated with a processor core and a plurality of programmable chip components;

means for configuring, at the generator module, the processor core and the plurality of programmable chip components for implementation on the programmable chip system, including creating a logic description and providing the logic description to a synthesis tool;

means for automatically determining voltage and ground pins associated with the programmable chip;

means for ~~providing a netlist, wherein~~ utilizing the generator module to automatically generate a netlist and automatically providing the netlist to a printed circuit board layout tool

which uses the netlist to generate a layout coupling the processor core and the plurality of programmable chip components to off-chip components; and

means for utilizing one or more secondary side arbitrators with one or more of the plurality of programmable chip components, thereby enabling direct communication between a secondary component to which a secondary side arbitrator corresponds and a primary programmable chip component; and

wherein the processor core transmits request controls to the secondary side arbitrator corresponding to the secondary component.

20. (Original) The apparatus of claim 19, wherein the netlist is a printer circuit board netlist.

21. (Currently Amended) The apparatus of claim 20, wherein capacitors are bypassed for ground pins ~~pints~~ and voltage pins.

22. (Original) The apparatus of claim 19, wherein the plurality of programmable chip components are received from a library.

23. (Original) The apparatus of claim 19, wherein customization information includes parameterization information.

24. (Original) The apparatus of claim 19, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

25. (Original) The apparatus of claim 19, wherein the off-chip component is an external memory device.

26. (Original) The apparatus of claim 19, wherein the off-chip component is an application specific standard product.